

CURRICULUM VITAE  
**Chi-Keung (CK) Luk**

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**I. PERSONAL DATA**

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**II. EMPLOYMENT HISTORY**

4/07 - present Senior Staff Engineer, Scalable Tools/Development Product Division/Software & Service Group (SSG), Intel.

1/03 - 3/07 Staff Systems Engineer, VSSAD (a research & advanced development group in computer architecture, compilers and systems), Digital Enterprise Group (DEG), Intel.

8/01 - 12/02 Senior Systems Engineer, VSSAD (a research & advanced development group in computer architecture, compilers and systems), Massachusetts Microprocessor Design Center (MMDC), Intel.

3/01 - 8/01 Principal Engineer, Alpha Development Group, Compaq.

3/00 - 2/01 Senior Engineer, Alpha Development Group, Compaq.

5/95 - 9/95 Summer Intern, TOBEY Compiler Group at the IBM Toronto Lab.

### III. EDUCATION

- Doctor of Philosophy in Compute Science, University of Toronto, January 2000.  
Dissertation: *Optimizing the Cache Performance of Non-Numeric Applications*.  
Supervisor: Todd C. Mowry.
- Visiting Scholar at the Compute Science Department in Carnegie Mellon University, November 1997-January 2000.
- Master of Philosophy in Compute Science, Chinese University of Hong Kong, July 1993.  
Dissertation: *Design and Implementation of a Multiparadigm Programming Language*  
Supervisor: Kam-Wing Ng.
- Bachelor of Science in Computer Science with First Class Honors, Chinese University of Hong Kong, May 1991.

### IV. HONORS & AWARDS

- Nominated for the ACM Dissertation Award in Computer Science by the University of Toronto, 2000 (only one nomination in a given year).
- 2007 Intel Achievement Award (for development of the Pin Dynamic Instrumentation System)
- Intel 2006 Digital Enterprise Group (DEG) Achievement Award (for Development of the Pin Dynamic Instrumentation System)
- Intel Departmental Award (for Optimization of Oracle with the ISpike Post-link Optimizer).
- Canadian Commonwealth Scholarship, 1994-1999 (around five selected in a given year by the Hong Kong Government for pursuing graduate studies in Canada).
- IBM Center for Advanced Studies Fellowship, 1995-1996, 1997-1998.
- Croucher Foundation Studentship, 1991-1993 (awarded by the Compute Science Department at The Chinese University of Hong Kong to the top two graduate students in a given year).
- Certificate of Merit of Excellent Teaching at The Chinese University of Hong Kong, 1993.

## V. MAJOR SOFTWARE DEVELOPED

- **The Qilin Parallel Programming System**
  - Founder of the Qilin project, a programming system for exploiting parallelism available on machines with a CPU and a GPU.
- **The Pin Dynamic Instrumentation System** (<http://www.pintools.org>).
  - Founder of the PinOS project, which extends Pin to whole-system instrumentation
  - Core developer of Pin
- **The Ispike Itanium Binary Optimizer**
  - Core developer for various profile-guided optimizations.

## VI. PATENTS

- Issued:
  - Chi-Keung Luk and Joel Emer. **Software-Controlled Pre-Execution in a Multithreaded Processor**, US Patent 7343602.
  - Chi-Keung Luk and Geoff Lowney. **Methods and Apparatus for Stride Profiling a Software Application**, US Patent 7181723.
- Filed:
  - Minjang Kim, Chi-Keung Luk, and Hyesoon Kim. **A Space-Efficient and Accurate Method to Detect Memory Dependences for the Purpose of Parallelization**.
  - Chi-Keung Luk and Geoff Lowney. **An Adaptive Compilation Technique for Scheduling Parallel Tasks on Heterogeneous Architectures**, US Patent filed December 2008.
  - Chi-Keung Luk and Robert Cohn. **Methods and Apparatus to Inline Conditional Instrumentation**, US Patent filed March 2006.
  - Chi-Keung Luk, Ady Tal, Robert Cohn, and Jonathan Beimel. **Optimizing Binary-level Instrumentation via Instruction Scheduling**, US Patent filed June 2005.
  - Chi-Keung Luk and Geoff Lowney. **Methods and Apparatus to Pre-execute Instructions on a Single Thread**, US Patent 20050050534, filed September 2003.
  - Chi-Keung Luk, Harish Patil, Robert Muth, Geoff Lowney, Robert Cohn, and Richard Weiss: **Profile-Guided Stride Prefetching**, US Patent 20020055964, filed October 2001.

## VII. PUBLICATIONS

### Refereed Conference Papers

[1] Minjang Kim, Hyesoon Kim, and Chi-Keung Luk. **How Can We Help Programmers to Make Parallel Programming Easier**. To appear in HotPar'2010, June 2010.

[2] Chi-Keung Luk, Sunpyo Sun, and Hyesoon Kim. **Qilin: Exploiting Parallelism on Heterogeneous Multiprocessors with Adaptive Mapping**. In *Proceedings of the 2009 ACM/IEEE International Symposium on Microarchitecture (MICRO)*, December 2009.

[3] Aamer Jaleel, Robert S. Cohn, Chi-Keung Luk, and Bruce Jacob. **CMP\$im: A Pin-based On-the-Fly Multicore Cache Simulator**. In *The Fourth Annual Workshop on Modeling, Benchmarking and Simulation (MoBS), co-located with ISCA'2008*.

[4] Prashanth Bungale and Chi-Keung Luk. **PinOS: A Programmable Framework for Whole-System Dynamic Instrumentation**. In *Proceedings of the 3<sup>rd</sup> ACM/USENIX International Conference on Virtual Execution Environment (VEE)*, pages 137-147, June 2007.

[5] Heidi Pan, Krste Asanovic, Robert Cohn, and Chi-Keung Luk. **Controlling Program Execution through Binary Instrumentation**. In *1st Workshop on Binary Instrumentation and Application (WBIA)*, September 2005.

[6] Chi-Keung Luk, Robert Cohn, Robert Muth, Harish Patil, Artur Klauser, Geoff Lowney, Steven Wallace, Vijay Janapa Reddi, and Kim Hazelwood. **Pin: Building Customized Program Analysis Tools with Dynamic Instrumentation**. In *Proceedings of the 2005 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 190-200, June 2005.

[7] Chi-Keung Luk, Robert Muth, Harish Patil, Robert Cohn, and Geoff Lowney. **Ispike: A Post-Link Optimizer for the Intel Itanium Architecture**. In *Proceedings of the 2<sup>nd</sup> International Conference on Code Generation and Optimization (CGO)*, pages 15-26, March 2004.

[8] Chi-Keung Luk, Robert Muth, Harish Patil, Geoff Lowney, Robert Cohn, and Richard Weiss. **Profile-Guided Post-Link Stride Prefetching**. In *Proceedings of the 2002 International Conference on Supercomputing (ICS)*, pages 167-178, June 2002.

[9] Dick Flower, Chi-Keung Luk, Robert Cohn, Geoff Lowney, Robert Muth, Harish Patil, and John Shakshober. **Kernel Optimizations and Prefetch with the Spike Executable Optimizer**. In *4<sup>th</sup> Workshop on Feedback-Directed and Dynamic Optimization (FDDO-4)*, December 2001.

[10] Chi-Keung Luk. **Tolerating Memory Latency Through Software-Controlled Pre-Execution in Simultaneous Multithreading Processors**. In *Proceedings of the 28<sup>th</sup> Annual International Symposium on Computer Architecture (ISCA)*, pages 40-51, July 2001.

[11] Chi-Keung Luk and Todd C. Mowry. **Memory Forwarding: Enabling Aggressive Layout Optimizations by Guaranteeing the Safety of Data Relocation**. In *Proceedings of the 26<sup>th</sup> Annual International Symposium on Computer Architecture (ISCA)*, pages 88-99, May 1999.

[12] Chi-Keung Luk and Todd C. Mowry. **Cooperative Prefetching: Compiler and Hardware Support for Effective Instruction Prefetching in Modern Microprocessors.** In *Proceedings of the 31<sup>st</sup> Annual International Symposium on Microarchitecture (MICRO)*, pages 182-193, December 1998.

[13] Todd C. Mowry and Chi-Keung Luk. **Predicting Data Cache Misses in Non-Numeric Applications Through Correlation Profiling.** In *Proceedings of the 30<sup>th</sup> Annual International Symposium on Microarchitecture (MICRO)*, pages 314-320, December 1997.

[14] Chi-Keung Luk and Todd C. Mowry. **Compiler-Based Prefetching for Recursive Data Structures.** In *Proceedings of the Seventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 222-233, October 1996.

[15] Chi-Keung Luk. **Memory Disambiguation for General-Purpose Applications.** In *Proceedings of the IBM CASCON 95*, November 1995.

[16] Kam-Wing Ng and Chi-Keung Luk. **An Integrated Computation Model for Parallel Programming.** In *Proceedings of IEEE TENCON 93/Beijing*, October 1993.

[17] Kam-Wing Ng and Chi-Keung Luk. **The Design of a Multiparadigm Programming Language I.** In *Proceedings of EuroMicro*, 1993 (published as a special issue in the *Journal of Systems Architecture* 37:171-174, 1993).

### **Referred Journal Articles**

[18] Moshe Bach, Mark Charney, Robert Cohn, Elena Demikhovskiy, Tevi Devor, Kim Hazelwood, Aamer Jaleel, Chi-Keung Luk, Gail Lyons, Harish Patil, and Ady Tal. **Analyzing Parallel Programs with Pin.** In *IEEE Computer*, 34-41, March 2010.

[19] Joel Emer, Pritpal Ahuja, Bathan Binkert, Roger Espasa, Toni Juan, Artur Klauser, Chi-Keung Luk Srilatha Manne, Shubhendu S. Mukherjee, Harish Patil, and Steven Wallace. **Asim: A Performance Model Framework.** In *IEEE Computer* 35(2): 68-76, February 2002.

[20] Chi-Keung Luk and Todd C. Mowry. **Architectural and Compiler Support for Effective Instruction Prefetching: A Cooperative Approach.** In *ACM Transactions on Computer Systems*, 19(1): 71-109, February 2001.

[21] Todd C. Mowry and Chi-Keung Luk. **Understanding Why Correlation Profiling Improves the Predictability of Data Cache Misses in Nonnumeric Applications.** In *IEEE Transactions on Computers*, 49(4), April 2000.

[22] Chi-Keung Luk and Todd C. Mowry. **Automatic Compiler-Inserted Prefetching for Pointer-Based Applications.** In *IEEE Transactions on Computers*, 48(2): 134-141, February 1999.

[23] Kam-Wing Ng and Chi-Keung Luk. **I+: A Multiparadigm Language for Object-Oriented Declarative Programming.** In *Computer Languages*, vol. 21, no 2, pp. 81-100, 1995.

[24] Kam-Wing Ng and Chi-Keung Luk. **A Survey of Languages Integrating Functional, Object-Oriented and Logic Programming.** In *Journal of Systems Architecture* (formerly *Microprocessing and Microprogramming*), 41:5-36, 1995.

## Poster Articles

[25] Prashanth Bungale and Chi-Keung Luk. **PinOS: A Programming Framework for Whole-System Dynamic Instrumentation**. In *VMWORLD 2007*, September 2007.

## Technical Reports and Dissertations

[26] Chi-Keung Luk. **Optimizing the Cache Performance of Non-Numeric Applications**. Ph.D. Thesis, Department of Computer Science, University of Toronto, January 2000. (*Nominated for the ACM Doctoral Dissertation Award*).

[27] Chi-Keung Luk and Todd C. Mowry. **Compiler and Hardware Support for Automatic Instruction Prefetching: A Cooperative Approach**. Carnegie Mellon University Technical Report CMU-CS-98-140, June 1998.

[28] Todd C. Mowry and Chi-Keung Luk. **Predicting Data Cache Misses in Non-Numeric Applications Through Correlation Profiling**. Carnegie Mellon University Technical Report CMU-CS-97-175, September 1997.

[29] Chi-Keung Luk. **The Design and Implementation of a Multiparadigm Programming Language**. Master Thesis, Department of Computer Science, The Chinese University of Hong Kong, July 1993.

## VIII. TEACHING EXPERIENCES

- **Ph.D. Committee Member**
  - i. Minjang Kim, Ph.D. Candidate of the Computer Science Department at Georgia Tech.
- **Interns Supervised**
  - Minjang Kim, Ph.D. Candidate of the Computer Science Department at Georgia Tech.
  - Prashanth Bungale, Ph.D. Candidate of the Computer Science Department at Harvard University.
  - Weihaw Chuang, Ph.D. from the Computer Science Department at University of California at San Diego.
- **Tutorial Organization and Presentations**
  - MIT Winter Break Class on *Using Pin for Computer Architecture and Software Research*, January 2007 (along with Aamer Jaleel, Harish Patil, Robert Cohn).
  - 2006 International Symposium of Computer Architecture (ISCA) Tutorial on *Using Pin for Computer Architecture Research* (along with Aamer Jaleel, Harish Patil, Bobbie Manne).
  - 2004 Architectural Support for Programming Languages and Operating Systems (ASPLOS) Tutorial on *Designing Instrumentation Tools with Pin* (along with Harish Patil, Wei Hsu, Dan Connor)

- 2004 Code Generation and Optimization (CGO) Tutorial on *Software Instrumentation and Hardware Profiling for Itanium Linux* (along with Robert Cohn and Stephane Eranian)
- **Teaching Assistant**
  - Department of Computer Science, University of Toronto, 1996.
  - Department of Computer Science, Chinese University of Hong Kong, 1991-1993.

## IX. PROFESSIONAL ACTIVITIES

- Program committee member for the *1<sup>st</sup> Workshop on Binary Instrumentation and Application* (WBIA) in conjunction with the PACT, September 2005
- Program committee member for the *1<sup>st</sup> Workshop on Memory System Performance* in conjunction with the *ACM International Conference on Programming Language Design and Implementation 2002*, Berlin, Germany, June 2002.
- Program committee member for the *34<sup>th</sup> Annual International Symposium on Microarchitecture (MICRO)*, Austin, Texas, December 2001.
- Member of ACM and IEEE

## X. REFERENCES

Dr. Todd C. Mowry  
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 Carnegie Mellon University  
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Dr. Joel S. Emer  
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 Intel Corporation  
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Dr. Geoff Lowney  
 Intel Fellow & CTO of the Intel SSG Developer's Product Division (DPD)  
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